UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,651	12/31/2001	Howard S. David	42390.P13872	9227

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EXAMINER
LI, ZHUO H

ART UNIT	PAPER NUMBER
2186	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 10/039,651	Applicant(s) DAVID, HOWARD S.
	Examiner Zhuo H Li	Art Unit 2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _31 December 2001_ .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-28_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-28_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4)☐ Interview Summary (PTO-413) Paper No(s). _____ .	
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5)☐ Notice of Informal Patent Application (PTO-152)	
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6)☐ Other:	

DETAILED ACTION

Specification

1.   The disclosure is objected to because of the following informalities:

Page 6 lines 4-5, "the DRAM is placed on a motherboard rather that on a memory

module" should be -- the DRAM is placed on a motherboard rather than on a memory

module--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999

(AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002

do not apply when the reference is a U.S. patent resulting directly or indirectly from an

international application filed before November 29, 2000. Therefore, the prior art date of the

reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA

35 U.S.C. 102(e)).

3. Claims 25-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumar et al. (US PAT. 6,247,094 hereinafter Kumar).

Regarding claim 25, Kumar discloses a method comprising delivering during a first plurality of transfer periods information corresponding to both an activate command, i.e., read or write access command from CPU to access the cache memory, and a cache fetch command, i.e., a cache fetch command via the way predictor (col. 8 lines 6-18), and delivering during a last transfer period information differentiating between an activate command and a cache fetch command, i.e., way predictor (70, figure 4) further compared the real hit or a miss with the signal generated from the tag array (55, figure 4), to performs memory access to the corresponding external cache data array (60, figure 4) and (col. 8 line 5 through col. 9 line 8 and col. 9 lines 31-48).

Regarding claim 26, Kumar discloses the method wherein delivering during a last transfer period information differentiating between an activate command and a cache fetch command includes delivering cache hit information, i.e., cache hit in the external cache data array (60, figure 4) or hit 0 which retrieve from the main memory (col. 8 line 5 through col. 9 line 8 and col. 9 lines 31-48).

Regarding claim 27, the limitations of the claim are rejected as the same reasons set forth in claim 25.

Regarding claim 28, the limitations of the claim are rejected as the same reasons set forth in claim 26.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et

al. (US PAT. 6,128,702 hereinafter Saulsbury) in view of Kumar et al. (US PAT. 6,247,094

hereinafter Kumar).

Regarding claim 1, Saulsbury discloses an apparatus (104, figure 2) comprising an array

of tag address storage locations, i.e., data cache bank tag/flag storage (col. 7 lines 42-61), and a

command sequencer and serializer unit, i.e., data cache bank logic (150, figure 2), coupled to the

array of tag address storage locations, the command sequencer and serializer unit to control a

data cache, i.e., data cache bank line storage (144, figure 2) associated with a memory module,

i.e., memory bank N (118, figure 2) and (col. 7 line 21 through col. 8 line 1), the command

sequencer and serializer unit to control the data cache associated with the memory module by

delivering a plurality of commands over a plurality of command and address lines, i.e., cache

line (4096), buffer control line, W/R control bus in figure 2. Saulsbury differs from the claimed

invention in not specifically teaches the commands delivered over a plurality of transfer periods,

the plurality of commands including an active command and a cache fetch command, the

activate and cache fetch commands differing in format only in the information delivered during a

last transfer period. However, Kumar teaches in the apparatus, i.e., CPU core (50, figure 4)

comprising a microprocessor, cache tag array (55, figure 4) and way predictor (70, figure 4), the

CPU core is able to accessing the external cache data array (60, figure 4) via the external bus (75,

figure 4) with commands and address in few clock cycles, i.e., the commands delivered over a

plurality of transfer periods, such us initiate stage, predict stage, fetch data array stage, compare

with tag array stage and retrieve information stage (col. 6 lines 32-46, figure 6 and col. 8 line 5

through col. 9 line 8), in addition, Kumar teaches when microprocessor initiates cache memory

read or write access, i.e., activate command, with request information to the cache tag array as

well as way predictor, and the way predictor based on it's history table and perform a lookup

function, if way predictor predicts a hit, it immediately forwards the way signal to the data array

and fetches the corresponding data, i.e., cache fetch command, further communicates with the

responses from tag array (col. 8 line 5 through col. 9 line 8 and col. 9 lines 35-60), furthermore,

Kumar also discloses, if the prefetch is hit in the way predictor, it contains not only the hit

information, but also the way/bank information, such as set or way information (col. 7 line 62

through col. 8 line 3). Therefore, it would have been obvious to a person of ordinary skill in the

art at the time the invention was made to modify the apparatus of Saulsbury is able to deliver a

plurality of command and address lines over a plurality of transfer periods, the plurality of

commands including an active command and a cache fetch command, the activate and cache

fetch commands differing in format only in the information delivered during a last transfer

period, as per teaching by the apparatus of Kumar, because it improves the overall efficiency of

the cache memory architecture, and lower latency, less circuitry, less power consumption, larger

data array size and faster front side snooping.

Regarding claim 2, Kumar discloses the activate command and the cache fetch command

differing in cache hit information delivered during the last transfer period (col. 8 line 5 through

col. 9 line 8 and col. 9 lines 35-60).

Regarding claim 3, Kumar discloses the cache fetch command further including way information delivered during the last transfer period (col. 7 line 62 through col. 8 line 42).

Regarding claim 4, Kumar discloses the plurality of commands each delivered over four transfer periods, i.e., initiate stage, predict stage, fetch data array stage, compare with tag array stage and retrieve information stage (figure 6 and col. 8 line 5 through col. 9 line 8).

Regarding claims 5-6, Kumar discloses the activate and cache fetch commands each including memory module destination information, i.e., way or bank information, during a first transfer period, i.e., predict stage from the way predictor, and the activate and cache fetch commands each including row address information during each of the four transfer periods, i.e., way predictor and tag array each comprising a number of entries which each entries comprising row address, i.e., index information of each corresponding data cache array (col. 6 line 58 through col. 8 line 3).

Regarding claim 7, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 8, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 9, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 10, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claims 11-12, the limitations of the claims are rejected as the same reasons set forth in claims 5-6.

Regarding claim 13, Saulsbury discloses an apparatus (104, figure 2) comprising at least

one memory device (118, figure 2), and a data cache, i.e., primary data cache bank (122, figure

2) coupled to the memory device via the cache line (4096) as drawn in figure 2. However,

Saulsbury differs from the claimed invention in not specifically teaches the data cache controlled

by a plurality of commands delivered by a memory controller component over a memory bus, the

memory controller component including an array of tag address storage locations, the commands

delivered over a plurality of transfer periods, the plurality of commands including an activate

command and a cache fetch command, the activate and cache fetch commands differing in

format only in the information delivered during a last transfer period. However, Kumar teaches

the data cache (60, figure 4), is controlled by the memory controller, i.e., CPU core (50, figure

4), via the memory bus (75, figure 4), with commands and address in few clock cycles, i.e., the

commands delivered over a plurality of transfer periods, such us initiate stage, predict stage,

fetch data array stage, compare with tag array stage and retrieve information stage (col. 6 lines

32-46, figure 6 and col. 8 line 5 through col. 9 line 8), and the memory controller is comprising a

tag array (55, figure 4), Kumar also teaches the memory controller comprising a way predictor,

and it is able to accessing the external cache data array (60, figure 4) via the external bus (75,

figure 4) with commands and address in few clock cycles (col. 6 lines 32-46), in addition, Kumar

teaches when microprocessor initiates cache memory read or write access, i.e., activate

command, with request information to the cache tag array as well as way predictor, and the way

predictor based on it's history table and perform a lookup function, if way predictor predicts a

hit, it immediately forwards the way signal to the data array and fetches the corresponding data,

i.e., cache fetch command, further communicates with the responses from tag array (col. 8 line 5

through col. 9 line 8 and col. 9 lines 35-60), furthermore, Kumar also discloses, if the prefetch is

hit in the way predictor, it contains not only the hit information, but also the way/bank

information, such as set or way information (col. 7 line 62 through col. 8 line 3). Therefore, it

would have been obvious to a person of ordinary skill in the art at the time the invention was

made to modify the apparatus of Saulsbury is able to deliver a plurality of command and address

lines over a plurality of transfer periods, the plurality of commands including an active command

and a cache fetch command, the activate and cache fetch commands differing in format only in

the information delivered during a last transfer period, as per teaching by the apparatus of

Kumar, because it improves the overall efficiency of the cache memory architecture, and lower

latency, less circuitry, less power consumption, larger data array size and faster front side

snooping.

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth

in claim 2.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth

in claim 3.

Regarding claim 16, the limitations of the claim are rejected as the same reasons set forth

in claim 4.

Regarding claims 17-18, the limitations of the claims are rejected as the same reasons set

forth in claims 5-6.

6.   Claims 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westberg

(US PAT. 5,361,391) and Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury), and

further in view of Kumar et al. (US PAT. 6,247,094 hereinafter Kumar).

Regarding claim 19, Westberg discloses a system (10, figure 1) comprising a processor

(12, figure 1), a memory controller (14, figure 1) coupled to the processor via the address bus

(22) and data bus (24), the memory controller including an array of tag address locations (30a

and 30b, figure 2 and col. 4 lines 34-46), and a command sequencer and serializer unit, i.e.,

control logic (28, figure 2) coupled to the array of tag address storage locations (col. 4 lines 34-

59), and memory module (16, figure 2) coupled to the memory controller via the address bus

(22), data bus (24) and control signal bus as show in figure 2, in addition, the memory controller

is able to provide a plurality of commands which including a read and preload command, i.e., the

memory controller further comprising a control logic (28, figure 2) which generates different

commands which received from the CPU to perform memory operations, and which including

read and pre-fetch commands (col. 4 line 6 through col. 5 line 66). Westberg differs from the

claimed invention in not specifically teaches the memory module including at least one memory

device and a data cache coupled to the memory device, the data cache controlled by a plurality of

commands delivered by the memory controller, the commands delivered over a plurality of

transfer periods, the plurality of commands including an activate command and a cache fetch

command, the activate and cache fetch commands differing in format only in the information

delivered during a last transfer period. However, Saulsbury discloses the computer system (100,

figure 1) comprising a memory device wherein the memory device including a plurality of

memory modules, i.e., memory block (104), and the memory module further including a memory

device, i.e., memory bank N (118) and a data cache (144) wherein the data cache coupled to the

memory device via the cache line bus (4096, figure 2), and the data cache controlled by

commands, i.e., cache line buses and buffer control buses (figure 2), delivered by the memory

controller, i.e., data cache bank logic (150) and (col. 7 lines 21-41 and col. 11 line 15 through

col. 12 line 6). In addition, Kumar teaches the data cache (60, figure 4), is controlled by the

memory controller, i.e., CPU core (50, figure 4), via the memory bus (75, figure 4), with

commands and address in few clock cycles, i.e., the commands delivered over a plurality of

transfer periods, such us initiate stage, predict stage, fetch data array stage, compare with tag

array stage and retrieve information stage (col. 6 lines 32-46, figure 6 and col. 8 line 5 through

col. 9 line 8), and the memory controller is comprising a tag array (55, figure 4), Kumar also

teaches the memory controller comprising a way predictor, and it is able to accessing the external

cache data array (60, figure 4) via the external bus (75, figure 4) with commands and address in

few clock cycles (col. 6 lines 32-46), Kumar further teaches when microprocessor initiates cache

memory read or write access, i.e., activate command, with request information to the cache tag

array as well as way predictor, and the way predictor based on it's history table and perform a

lookup function, if way predictor predicts a hit, it immediately forwards the way signal to the

data array and fetches the corresponding data, i.e., cache fetch command, further communicates

with the responses from tag array (col. 8 line 5 through col. 9 line 8 and col. 9 lines 35-60),

furthermore, Kumar also discloses, if the prefetch is hit in the way predictor, it contains not only

the hit information, but also the way/bank information, such as set or way information (col. 7

line 62 through col. 8 line 3). Therefore, it would have been obvious to a person of ordinary skill

in the art at the time the invention was made to modify the system of Westberg in having the

memory module including at least one memory device and a data cache coupled to the memory

device, the data cache controlled by a plurality of commands delivered by the memory controller,

the commands delivered over a plurality of transfer periods, the plurality of commands including

an activate command and a cache fetch command, the activate and cache fetch commands

differing in format only in the information delivered during a last transfer period, as per teaching

of the combination of Saulsbury and Kumar, because it improves the overall efficiency of the

cache memory architecture, and lower latency, less circuitry, less power consumption, larger data

array size and faster front side snooping.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth

in claim 2.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth

in claim 3.

Regarding claim 22, the limitations of the claim are rejected as the same reasons set forth

in claim 4.

Regarding claims 23-24, the limitations of the claims are rejected as the same reasons set

forth in claims 5-6.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Tran (US PAT. 5,900,012) discloses storage device having varying access times and a

superscalar microprocessor employing the same (abstract).

8.   Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington, VA, Fourth Floor (Receptionist).

9.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The

examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The

examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li
Art Unit 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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